D. Remarks

Objections to Claims.

Claims 10-11 have been amended as suggested by the Examiner to address the claim objections.

Rejection of Claims 1-20 Under 35 U.S.C. §102(e) based on *Miller* (U.S. Patent No. 6,181,164).

The rejection of claims 1-14 will first be addressed.

The invention of claim 1 is directed to an integrated circuit device that includes a programmable portion comprising a plurality of circuits configurable by a user of the integrated circuit device. The integrated circuit device also includes at least one communication portion comprising at least one circuit block manufactured to perform a predetermined data communication function including converting received first data values into second data values.

As is well established, anticipation requires the presence of a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. There must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention.[1]

The cited reference *Miller* does not show all the limitations of claim 1. *Miller* shows linear feedback shift registers (LFSRs), and related circuits, configured in a programmable gate array (PGA). That is, the reference never shows "at least one circuit block manufactured to perform a predetermined data communication function". In all cases, *Miller* teaches circuits formed by configuring programmable circuits into various blocks. That is, the circuits described by *Miller* are not manufactured to provide any particular function, but are programmable -- and hence do not provide any realizable function. It is only after the circuits of the PGA have been configured that any particular function is provided:

> The present invention generally relates to linear feedback shift registers, and more particularly to ***a programmable gate array implementation of a linear feedback shift register***. (*Miller*, Col. 1, Lines 13-15, emphasis added).

In various embodiments, the invention comprises a linear feedback shift register

[1] Scripps Clinic & Research Found. v. Genetech Inc., 18 USPQ 2d 1001, 1010 (Fed. Cir. 1991).

> *in* a programmable logic device. A first lookup table ***is configured*** as a shift register having n selectable taps and a shift-input. A second lookup table ***is configured*** as a parity generator... (*Miller*, Col. 1, Line 66 to Col. 2, Line 4, emphasis added).

> [A]n appreciation of the present invention is presented by way of specific examples, in this instance, embodiments of the invention ***as applied to a programmable gate array having 4-input LUTs***. (*Miller*, Col. 3, Lines 42-45, emphasis added).

The various components of the LFSRs and related circuits are uniformly implemented with programmable (e.g., PGA) components, and thus cannot be considered to be "manufactured to perform a predetermined data communication function including converting received first data values into second data values", as recited in claim 1. A few examples of this are set forth below, but it is understood that these explicit teaching occurs throughout the reference:

> In an example implementation... parity generator 104 ***is implemented with a programmable array lookup table*** having an output coupled to the input of first stage 106 of shift register 102. (*Miller*, Col. 4, Lines 33-37, emphasis added).

> LFSR 200 includes respective shift registers... implemented in accordance with the teachings of the co-pending patent application by Bauer entitled, "LOOKUP TABLES WHICH DOUBLE AS SHIFT REGISTERS,"... Thus... shift registers 202-208 ***are implemented using 4-input LUTs***... (*Miller*, Col. 4, Lines 58-66, emphasis added).

> [T]he present invention provides, among other aspects, an LFSR ***implemented in a programmable gate array in a manner that makes efficient use of the programmable resources***. (*Miller*, Col. 11, Lines 36-38, emphasis added).

Applicants believe examination of the FPGA referred to in *Miller* makes the above teachings even clearer. *Miller* specifically refers to implementing the LFSR (and related circuits) in a Virtex™ FPGA of Xilinx, Inc.:

> Thus in one example embodiment of an LFSR... the Virtex FPGA from XILINX, a 16-stage shift register can be ***implemented with a 4-input LUT***. (*Miller*, Col. 11, Lines 36-38, emphasis added).

> In an example embodiment using the Virtex FPGA from XILINX... shift register 254 and flip-flop 272 cannot be mapped to the same slice. However, it will be appreciated that LFSR 250 ***can be mapped to two slices of a Virtex CLB***... [CLB stands for "configurable logic block"] (*Miller*, Col. 7, Lines 56-63, emphasis added).

Applicants have attached hereto a copy of a product specification for a Virtex™ FPGA of Xilinx, Inc. (see Exhibit A). The same or similar data is believed to have been incorporated into the cited reference. The information presented in Exhibit A shows that the Virtex™ device does not have any circuit blocks "manufactured to perform a predetermined data communication function including converting received first data values into second data values", as recited in claim 1. The device includes configurable logic blocks (CLBS).

Thus, the specific examples shown in *Miller* are believed to teach away from Applicants' invention by showing circuits blocks manufactured for no specific function (being entirely formed from programmable resources), that are subsequently configured as LFSRs and related types of circuits.

For these reasons, the cited reference does not show or suggest all the limitations of claim 1, and this ground for rejection is traversed.

Various claims depending from claim 1 are believed to be separately patentable over the cited reference.

Claim 5, which depends from claim 1, recites that the integrated circuit device includes a plurality of input/outputs commonly connected to a programmable portion and a communication portion. Such an arrangement is not shown in the cited referenced.

Miller only shows programmable resources. Accordingly, the reference does not show inputs to both a programmable portion and a communication portion. Further, the rejection is not believed to have shown anticipation. To show the limitations of claim 5, the rejection relies on the following portions of the reference:

As per claim 5, the input/output port is at least described in col. 6, lines 12-32. (Office Action, dated 11/17/2004, Page 3, Line 20).

Applicants respectfully request clarification of this ground for rejection. The above-cited portion describes an LFSR configured from two look up tables (LUTs) (one configured into a shift register, the other to provide an XOR function). There appears to be no description of one, let alone multiple I/Os commonly connected to both programmable and communication portions of the same integrated circuit device.

Accordingly, because the cited reference is not believed to show all the limitations claim 5, this claim is believed to be separately patentable.

Claim 9, which depends from claim 1 (by way of intermediate claim 6), recites that the communication portion further includes "an operational control store that provides one of a plurality of operational values to the data operation circuits that controls the type of operation performed on the received data". This is not shown in the cited reference.

Multiple operational values are never shown in any of the embodiments of *Miller*. Applicants will attempt to demonstrate this by briefly describing various embodiments, and showing each provides <u>one</u> function.

FIG. 1 of *Miller* shows an LFSR operating according to the polynomial $g(x) = 1+X^1+X^2+X^7+X^{16}$. There is never any mention of a store or similar circuit for changing the operation of the LFSR. FIG. 2 of *Miller* shows an LFSR with selectable taps. However, taps are <u>programmed</u> values. Thus, the LFSR provides a (singular) function, as explicitly noted:

> In a programmable gate array embodiment, the selection signals can be programmable, thereby providing the capability to implement ***a*** different polynomial if desired. (*Miller*, Col. 4, Lines 46-48, emphasis added).

FIG. 3 of *Miller* shows an 8-stage LFSR operating according to a particular polynomial. As in the case of FIG. 2, the reference notes how the arrangement can be reconfigured to accommodate different functions, but does not show any sort of store for multiple operational values, as recited in claim 9. FIGS. 4 and 5 show approaches based on time-multiplexed LUTs. Such examples again show <u>single</u> functions and are completely lacking an "operational store" as recited in claim 9.

Applicants believe the above showing, at a minimum, demonstrates that rejection has not met the necessary burden of proof, as no feature has been show to correspond to Applicants' "operational control store". The remaining embodiments do not show such a feature, and will be addressed upon final rejection and/or appeal.

Claim 11, which depends from claim 9, recites that the operational control store includes circuits that can provide a user operational value and a preset operational values established by at least one integrated circuit manufacturing step. Through the claim dependencies, it is understood that "operational values" recited in claim 9 control the type of operation performed on received data within the communication portion.

The reference *Miller* teaches programmable elements of a PGA, including programmable 4-input LUTs. However, such LUTs must be configured in order to provide any function. The rejection of claim 11 cites column 5 of *Miller* to reject claim 11. However, this portion of the reference is clearly referring to LUTs that have already been configured in one particular arrangement as shift registers according to user data. No alternative configuration is shown via an operational value provided by some store.

Accordingly, because the cited reference is not believed to show all the limitations claim 11, this claim is also believed to be separately patentable.

The rejection of claims 15-20 will now be addressed.

The invention of claim 15 is directed to a semiconductor device that includes a programmable logic device having a communication portion embedded therein. The communication portion includes non-programmable circuits designed to provide a selectable data communication function.

The cited reference *Miller* teaches the formation of LFSR and related functions utilizing programmable circuits. Accordingly, the reference cannot show all the limitations of claim 15. More particularly, *Miller* discloses the utilization of look-up tables (LUTs) for assorted sections of LFSRs. However, as emphasized above in conjunction with claim 1, such LUTs are programmable and configured to provide specific functions (e.g., shift registers, multiplexers, XOR functions, etc.).

Thus, because the various circuits of *Miller* are implemented with programmable resources, not only does the reference not show the limitations of claim 15, the reference is believed to teach away from non-programmable circuits as recited in claim 15.

For these reasons, the cited reference does not show or suggest all the limitations of claim 15, and this ground for rejection is traversed.

Various claims depending from claim 15 are believed to be separately patentable over the cited reference.

Claim 16, which depends from claim 15, recites that the communication portion includes circuit blocks that provide a different communication function. Such an arrangement is not shown or suggested by the cited reference.

The reference would appear to teach away from Applicants' claim 16 limitation. *Miller* teaches a PGA with same programmable function blocks: 4-input programmable LUTs. These programmable LUTs, absent any user programming, provide the same function.

Thus, because the reference does not appear to show separate circuit blocks providing different data communication functions, all the limitations of claim 16 are not shown in the reference, and this ground for rejection is traversed.

Claim 18, which depends from claim 15, recites that the communication portion includes two particular circuits (1) a block converter circuit that encodes data input words into output data words, and (2) a scrambler circuit that scrambles data values according to an operational control value. *Miller* does not show or suggest an arrangement with two such circuit blocks.

Miller does not show a scrambler circuit. *Miller* teaches a long scrambling code generator, but no scrambler circuit. As is well understood by those skilled in the art, a scrambler circuit can scramble data according to a scramble code (e.g., multiply or modulo operation). Thus, *Miller* only shows the generation of a code value that can be utilized by a scrambler circuit, not a scrambler circuit itself.

For this reason alone, the ground for rejection is traversed.

In addition or alternatively, *Miller* never shows multiple circuits in the same portion of semiconductor device. *Miller* only teaches individual circuits implemented in a PGA.[2]

For all of these reasons, claim 18 is believed to be separately patentable over the cited reference.

Claim 19, which depends from claim 15, recites that the communication portion includes two particular circuits (1) a block converter circuit that encodes data input words into output data words, and (2) a de-scrambler circuit that de-scrambles data values according to an operational control values.

[2] See *Miller*, all figures. None of the circuits shown is ever shown or suggested to form one part of a section containing other different circuits.

Miller does not show or suggest de-scrambling. A word search of the reference shows that de-scrambling is never described. Because *Miller* provides no teaches related to de-scrambling, the reference cannot show all the limitations of claim 19.

Accordingly, claim 19 is separately patentable over the cited reference.

Claim 20, which depends from claim 18, recites that the communication portion includes an operational control store that provides selectable operational control values to scrambler circuit.

To address this ground for rejection, Applicant incorporates by reference herein, the comments set forth above for claim 9.

Rejection of Claims 21 and 23 Under 35 U.S.C. §102(e) based on *Killian et al.* (U.S. Patent Publication No. 2003/0208723A1).

The invention of claim 21 is directed to a method that includes performing predetermined logic functions on a programmable logic portion of an integrated circuit and performing serial data communication functions on a communication portion of *the* integrated circuit. The communication portion includes circuit blocks that are not synthesized with programmable logic device configuration data.

The cited reference does not show the limitations of claim 21.

Claim 21 is directed to a method where both steps are executed on the same integrated circuit. The reference *Killian et al.* is not related to a single integrated circuit. *Killian et al.* teaches a system and method for designing a configurable processor. The system teaches an emulation board. This board includes many separate components:

> [0285] It is preferable that the system make available hardware processor emulation as well as software processor emulation. For this purpose, the preferred embodiment provides an ***emulation board***. As shown in FIG. 6, the ***emulation board*** 200 uses a complex programmable logic device 202... (*Killian*, Page 18).

> [0287] The emulation board 200 has several resources... the CPLD device 202 itself, EPROM 204, SRAM 206, synchronous SRAM 208, flash memory 210 and two RS232 serial channels 212... (*Killian*, Page 18).

It is clear the complex programmable logic device (CPLD), ERPROM, SRAM, synchronous SRAM, flash memory, and two RS232 serial channels are separate components of the same board. Accordingly, the serial channels do not perform data communication functions on the same integrated circuit as the programmable logic portion.[3]

Because the cited reference does not show or suggest all the limitations of claim 21, this ground for rejection is traversed.

Rejection of Claim 22 Under 35 U.S.C. §103(a) based on *Killian et al.* in view of *Miller*.

To the extent that this ground for rejection relies on the reference to show limitations of base claim 22, the comments set forth above for claim 21 are incorporated by reference herein. More particularly, because *Killian* does not show or suggest "performing serial data communication functions on a communication portion of the integrated circuit", a prima facie case of obviousness has not been established.

Claims 10 and 11 have been amended, not in response to the cited art, but to address objections related to form.

The present claims 1-23 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

02/08/05

Bradley T. Sako
Attorney
Reg. No. 37,923

Bradley T. Sako
WALKER & SAKO, LLP
300 South First Street
Suite 235
San Jose, CA 95113
Tel. 1-408-289-5315

[3] See *Killian et al.*, FIGURE 8 and paragraphs [0285] to [0287].